PIPELINED ARCHITECTURE FOR IMPLEMENTING RECURSION PROCESSES

ABSTRACT

A method and apparatus for performing a recursion process on a data block for error correction. The disclosure describes concurrently operating pipelined sub-processes that decode the data block with error correction. The pipelined sub-processes are implemented as sub-circuits of an integrated circuit. The output data from each sub-process is stored for input by a subsequent sub-process of the pipelined sub-processes.